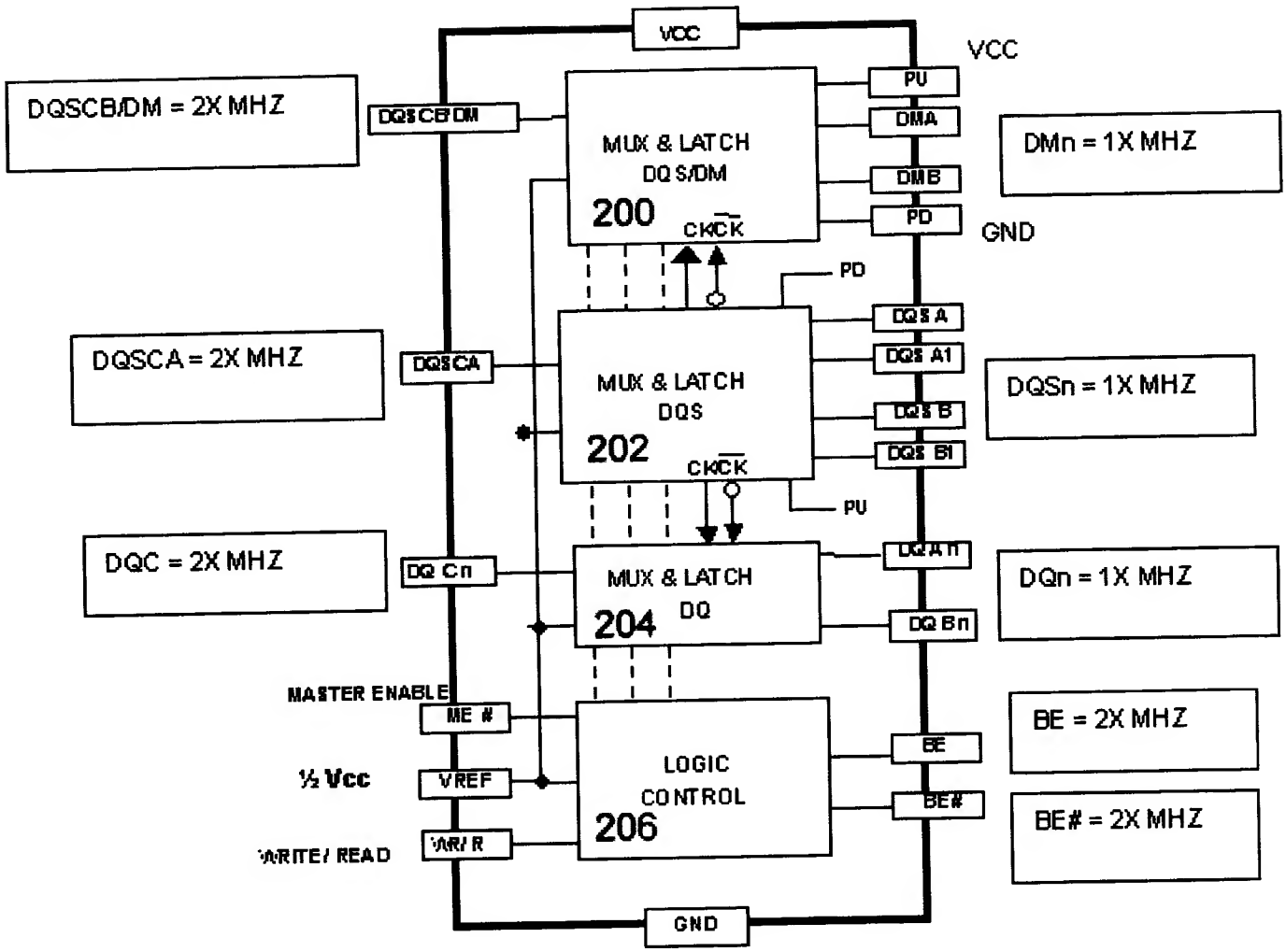

VCC
VCC
DQSCB/DM = 2X MHZ
DQSCB/DM
MUX & LATCH
DQS/DM
200
CK/CK
PU
DMA
DMB
PD
DMn = 1X MHZ
GND
PD
DQSCA = 2X MHZ
DQSCA
MUX & LATCH
DQS
202
CK/CK
DQS A
DQS A1
DQS B
DQS B1
DQSn = 1X MHZ
PU
DQC = 2X MHZ
DQ Cn
MUX & LATCH
DQ
204
DQ An
DQ Bn
DQn = 1X MHZ
MASTER ENABLE
ME #
½ Vcc
VREF
WRITE/ READ
WR/ R
LOGIC
CONTROL
206
BE
BE#
BE = 2X MHZ
BE# = 2X MHZ
GND

Figure 1

Figure 2

FUNCTION TABLE

DISABLED DIMM

INPUT			INPUT / OUTPUT					Internal Latch Outputs		OUTPUT				Operating Mode
ME #	WR	BE CLK	C[n]	B[n]	A[n]	DQS CA	DQSCB DM	Q10[n] (A)	Q9[n] (B)	DMA	DMB	DQSA DQSA1	DQSB DQSB1	
1	X	X	Hi - Z	Hi - Z	Hi - Z	Hi - Z	Hi - Z	No change	No change	No change	No change	Hi - Z	Hi - Z	Disable DIMM

READ CYCLES

INPUT					Internal Latch Outputs		OUTPUT							Operating Mode
ME #	WR	BE CLK	B[n]	A[n]	Q10[n] (A)	Q9[n] (B)	C[n]	DQS CA	DQSCB DM	DMA	DMB	DQSA DQSA1	DQSB DQSB1	
0	1	↓	Input	Input	A[n]	No change	Q10(A)	PU	PD	Don't Care	Don't Care	Hi - Z	Hi - Z	C Read A
		0			No change	No change								
0	1	↑	Input	Input	No change	B[n]	Q9 (B)	PD	PU	Don't Care	Don't Care	Hi - Z	Hi - Z	C Read B
		1			No change	No change								

WRITE CYCLES *(DQ and DM lines)*

INPUT						Internal Latch Outputs				OUTPUT				Operating Mode
ME #	WR	BE CLK	DQS CA	DQSCB DM	C[n]	Q10[n] (A)	Q9[n] (B)	Q19(A)	Q20(B)	A[n]	B[n]	DMA	DMB	
0	0	X	↑	Input	Input	C[n]	No change	DM	No change	Q10 (A)	Q9 (B)	Q19(A)	Q20(B)	C Write Q10(A) Send DQSB
0	0	X	↓	Input	Input	No change	C[n]	No change	DM	Q10 (A)	Q9 (B)	Q19(A)	Q20(B)	C Write Q9(B) Send DQSA

WRITE CYCLES (DQS Counter)

INPUT				Internal Latch Outputs		OUTPUT		Operating Mode
ME #	WR	BE CLK	DQS CA	Q28(A)	Q27(B)	DQSA DQSA1	DQSB DQSB1	
1	X	X	X	0	0	Hi - Z	Hi - Z	Disable DIMM *(DQS latch reset)*
0	1	X	X	0	0	Hi - Z	Hi - Z	Read Cycle *(DQS latch reset)*
0	0	X	First ↑	No change	No change	Q28(A)	Q27(B)	C Write DQ *(1st Write Cycle)*
0	0	X	↑ (All subsequent)	No change	Toggle	Q28(A)	Q27(B)	C Write DQ Send DQSB
0	0	X	↓	Toggle	No change	Q28(A)	Q27(B)	C Write DQ Send DQSA

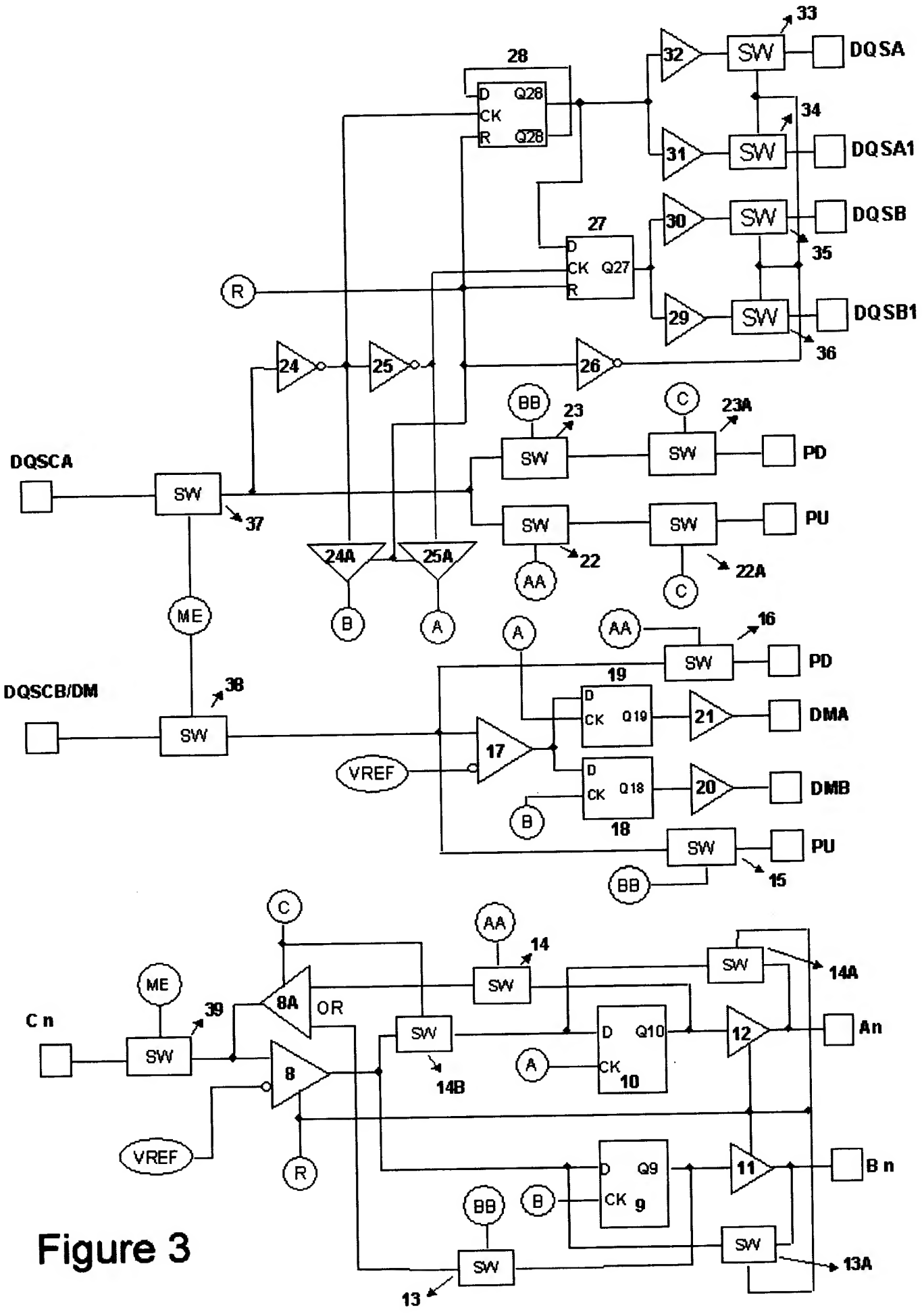

33
32
SW
DQSA
28
D Q28
CK
R Q28
34
31
SW
DQSA1
30
SW
DQSB
27
D
CK Q27
R
35
R
29
SW
DQSB1
36
24
25
26
BB
23
C
23A
SW
SW
PD
DQSCA
SW
37
SW
SW
PU
24A
25A
22
22A
AA
C
ME
B
A
A
AA
16
SW
PD
19
38
DQSCB/DM
D
CK Q19
21
DMA
SW
17
VREF
D
CK Q18
20
DMB
B
18
SW
PU
BB
15
C
AA
14
SW
SW
14A
ME
8A
OR
C n
39
SW
SW
D Q10
12
An
8
14B
A
CK
10
VREF
R
D Q9
11
B n
BB
B
CK 9
SW
SW
13A
13

Figure 3

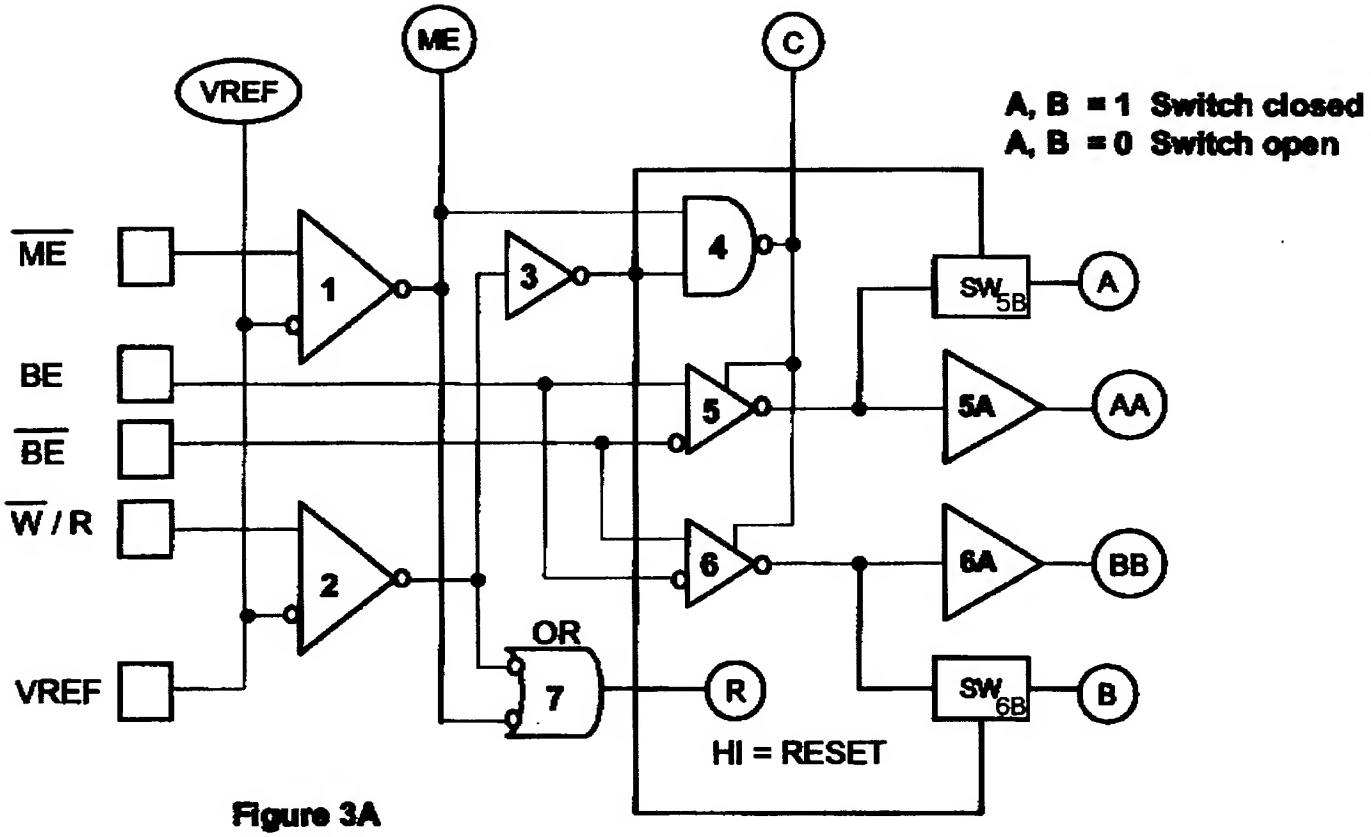

ME
C
VREF
A, B = 1 Switch closed
A, B = 0 Switch open
ME
BE
BE
W / R
VREF
1
2
3
4
5
6
7
OR
SW5B
SW6B
5A
6A
A
AA
BB
B
R
HI = RESET

Figure 3A

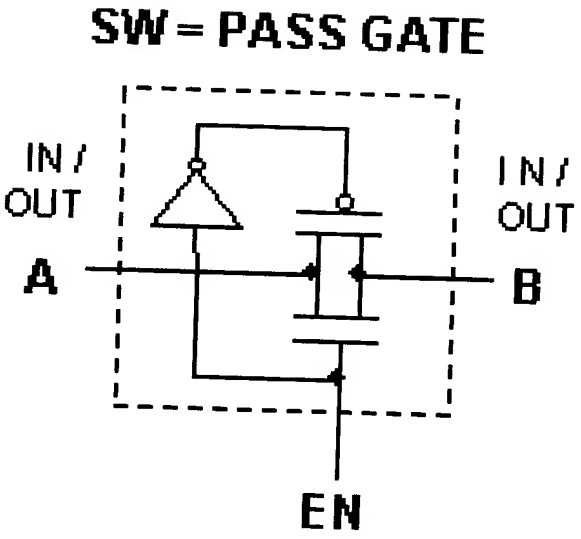
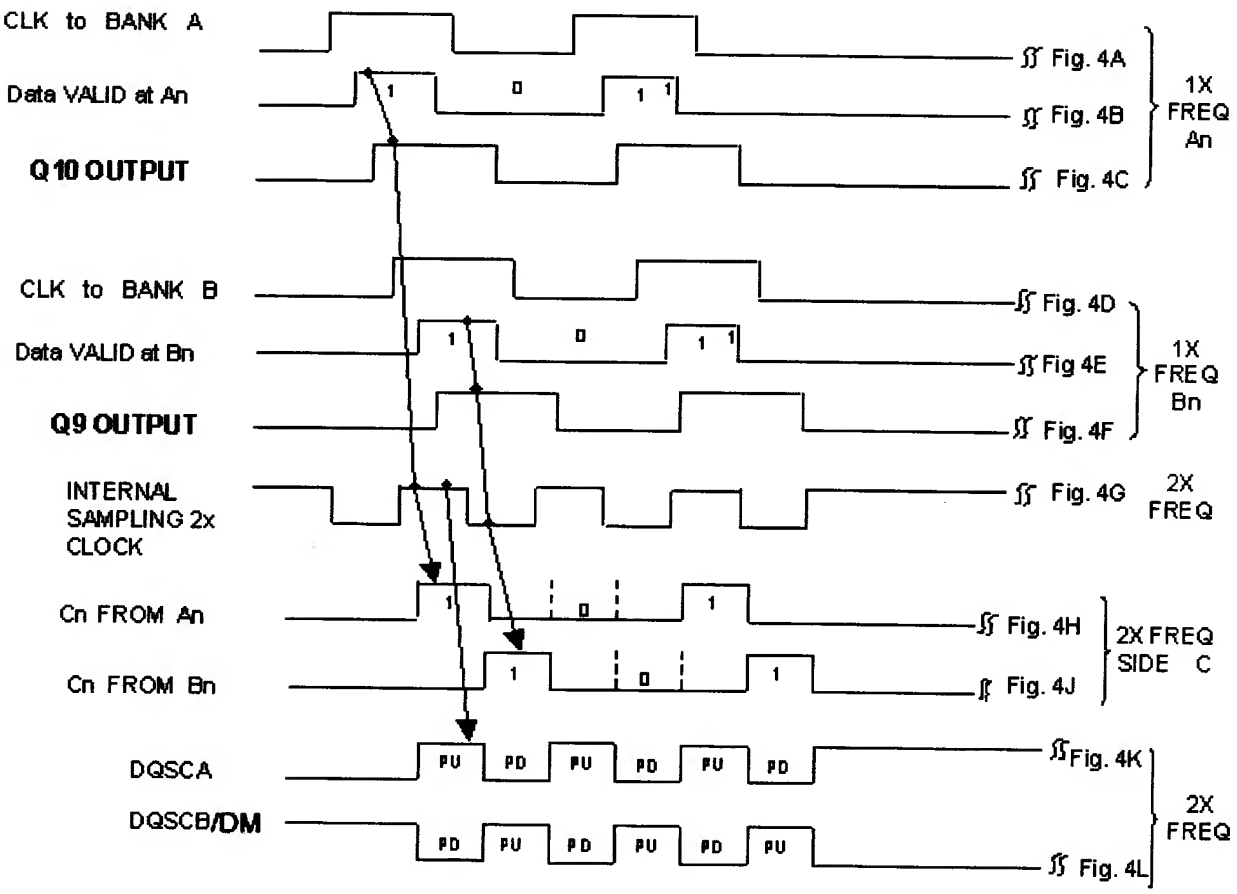
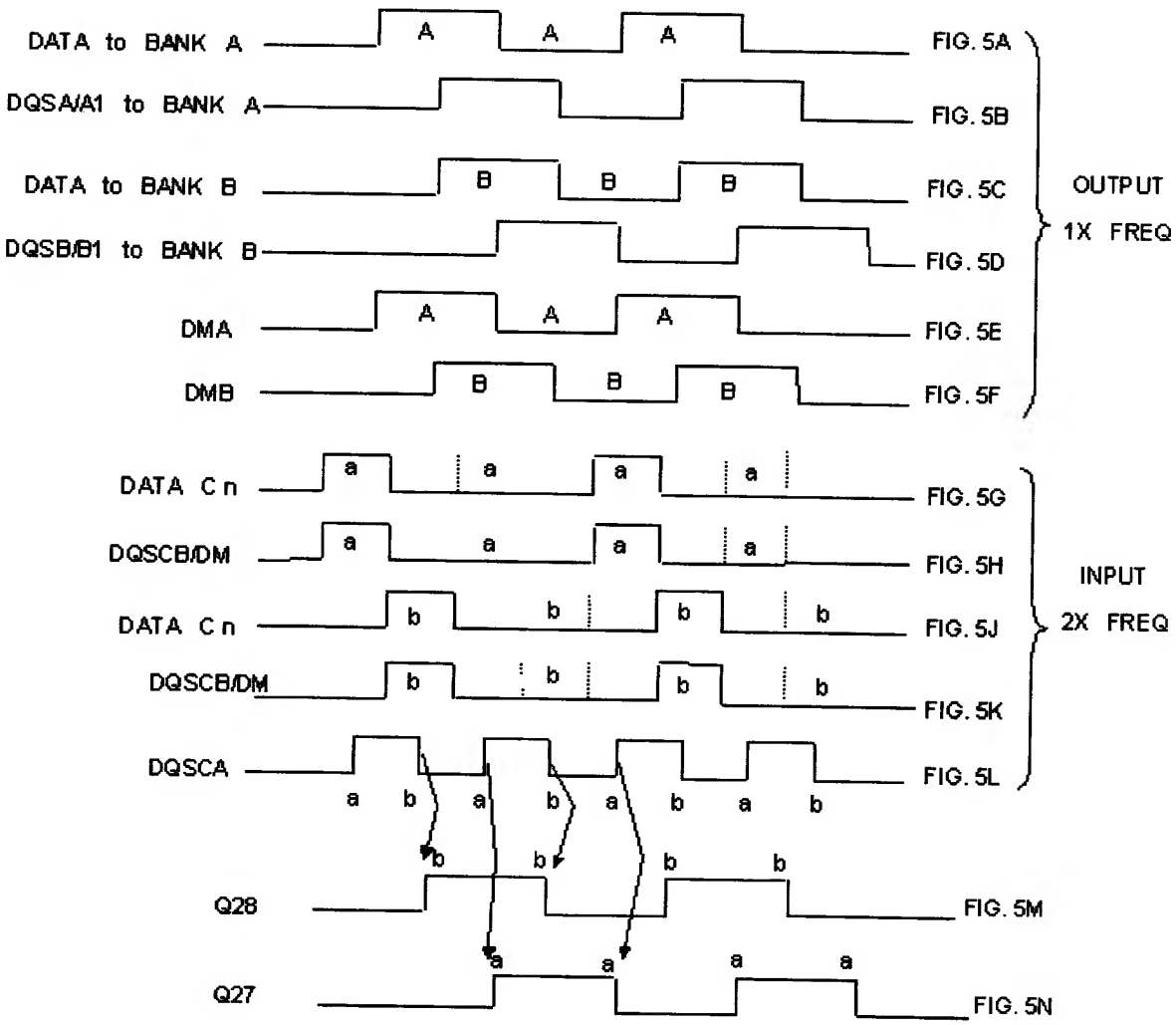


Figure 3B



READ OP (DATA FROM An, Bn to Cn)

Figure 4



WRITE OP (DATA from Cn to An, Bn)

Figure 5

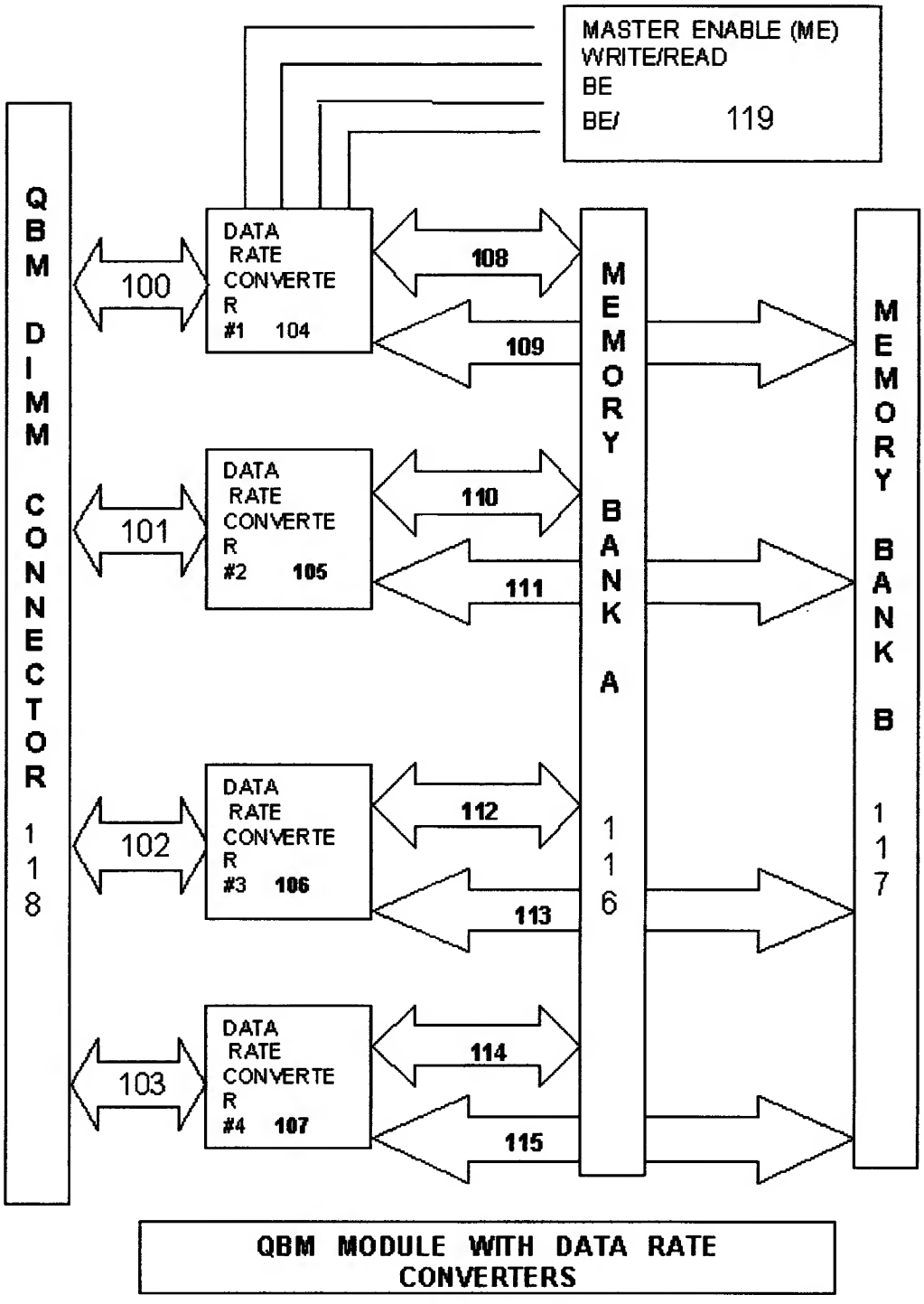

MASTER ENABLE (ME)
WRITE/READ
BE
BE/
119
QBM DIMM CONNECTOR 118
100
101
102
103
DATA RATE CONVERTER #1 104
DATA RATE CONVERTER #2 105
DATA RATE CONVERTER #3 106
DATA RATE CONVERTER #4 107
108
109
110
111
112
113
114
115
MEMORY BANK A 116
MEMORY BANK B 117
QBM MODULE WITH DATA RATE CONVERTERS

Figure 6